COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR IMAGE SENSORS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of U.S. application Ser. No. 14/830,181, filed Aug. 19, 2015, which claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2014-0107842, filed on Aug. 19, 2014, in the Korean Intellectual Property Office, the entire contents of which are hereby incorporated by reference.

BACKGROUND

[0002] Exemplary embodiments of the inventive concept relate to a complementary metal-oxide-semiconductor (CMOS) image sensor, and in particular, to CMOS image sensors with improved optical characteristics.

[0003] An image sensor is a device that converts optical images into electrical signals. With increased development of the computer and communications industries, there is an increased demand for high performance image sensors in a variety of applications such as digital cameras, camcorders, personal communication systems, gaming machines, security cameras, micro-cameras for medical applications, and/or robots.

[0004] The image sensors may be generally classified into charge coupled device (CCD) and complementary metal-oxide semiconductor (CMOS) image sensors. The CMOS image sensors are operated using a simple operation method and are configured to have signal processing circuits integrated on a single chip, and thus, CMOS image sensors make it possible to realize products including scaled CMOS image sensors. In addition, CMOS image sensors may operate with relatively low consumption power, and thus, they are applicable to portable electronic devices. Furthermore, CMOS image sensors can be fabricated using cost-effective CMOS fabrication techniques and can provide high resolution images. Accordingly, the use of CMOS image sensors has increased.

SUMMARY

[0005] Exemplary embodiments of the inventive concept provide CMOS image sensors with improved optical characteristics.

[0006] According to an aspect of an exemplary embodiment, there is provided a complementary metal-oxide-semiconductor (CMOS) image sensor that may include an epitaxial layer having a first conductivity type and having a first surface and a second surface facing each other; a first device isolation layer extending from the first surface to the second surface of the epitaxial layer to define a first pixel region and a second pixel region; a well impurity layer of a second conductivity type formed adjacent to the first surface and formed in the epitaxial layer of each of the first and second pixel regions; a second device isolation layer formed in the well impurity layer in each of the first and second pixel regions to define a first active portion and a second active portion which are spaced apart from each other in each of the first and second pixel regions; first and second transfer gates disposed on the first active portions of the first and second pixel regions, respectively; first and second floating diffusion regions formed in the first active portions and beside the first and second transfer gates, respectively; and a connection line crossing over the first and second pixel regions and being connected to both the first and second floating diffusion regions.

[0007] In some exemplary embodiments, in the epitaxial layer, a doping concentration of impurities of the first conductivity type may decrease in a direction from the first surface toward the second surface.

[0008] In some exemplary embodiments, the epitaxial layer may comprise a first epitaxial layer having a first doping concentration, a second epitaxial layer having a second doping concentration different from the first doping concentration, and a third epitaxial layer having a third doping concentration different from the second doping concentration.

[0009] In some exemplary embodiments, the first epitaxial layer may be adjacent to the second surface, the third epitaxial layer may be adjacent to the first surface, and the second epitaxial layer may be disposed between the first and third epitaxial layers, and the first doping concentration may be lower than the second doping concentration, and the second doping concentration may be lower than the third doping concentration.

[0010] In some exemplary embodiments, the CMOS image sensor may comprise a potential barrier layer having the second conductivity type and enclosing a sidewall of the first device isolation layer, and a doping concentration of impurities of the second conductivity type may be higher in the potential barrier layer than in the well impurity layer.

[0011] In some exemplary embodiments, the first device isolation layer may comprise an insulating layer extending from the first surface to the second surface of the epitaxial layer, and the epitaxial layer may be in direct contact with the insulating layer.

[0012] In some exemplary embodiments, a width of the first device isolation layer may decrease in a direction from the first surface toward the second surface.

[0013] In some exemplary embodiments, a width of the first device isolation layer may increase in a direction from the first surface toward the second surface.

[0014] In some exemplary embodiments, the first device isolation layer may comprise an insulating layer extending from a bottom surface of the second device isolation layer to the second surface of the epitaxial layer, the insulating layer having an air gap formed therein.

[0015] In some exemplary embodiments, the first device isolation layer may comprise a first insulating layer being in contact with the epitaxial layer and having a refractive index lower than that of the epitaxial layer; and a second insulating layer having a refractive index different from that of the first insulating layer.

[0016] In some exemplary embodiments, the CMOS image sensor may further comprise a first logic transistor formed on the second active portion of the first pixel region; and a second logic transistor formed on the second active portion of the second pixel region, and the connection line may electrically connected to a drain electrode of the first logic transistor and a gate electrode of the second logic transistor.

[0017] In some exemplary embodiments, the CMOS image sensor may further comprise a third logic transistor formed on the second active portion of the second pixel region, and the third logic transistor may be connected in series to the second logic transistor.